Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

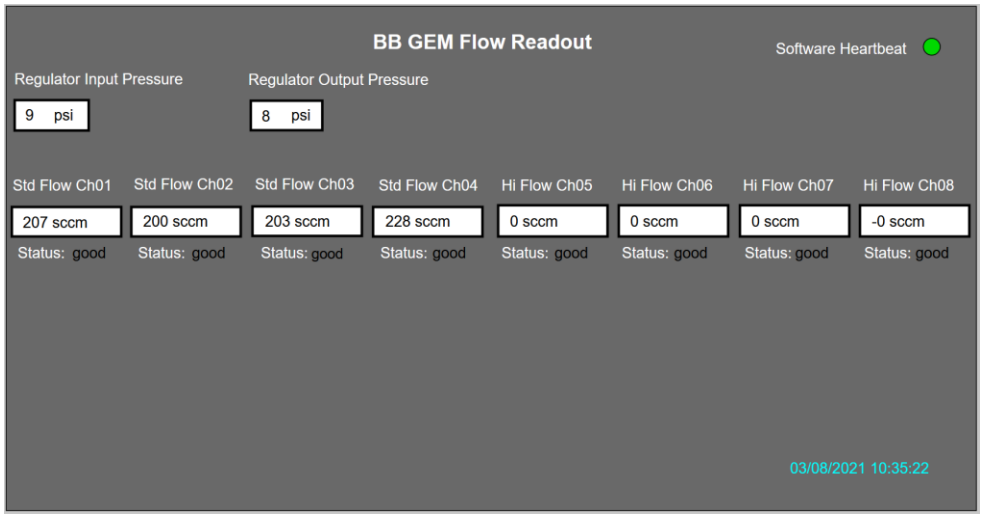
Weekly Report, 2021-03-10

Summary

Hall A – GEM

Peter Bonneau, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Installed mezzanine extension board on the BigBite gas distribution Raspberry Pi
- Added input and output regulator pressure transducers to WEDM readout display



BigBite GEM flow readout display with pressure transducer readings

- Cut, terminated, tested, and labeled 48 BNC-to-LEMO cables; 240 of 272 complete

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Mindy Leffel, Marc McMullen

- Wrote PLC code for Radial Support Upstream interlock
  - ✶ Added Add-On instruction to compare readout with set limits entered by user
  - ✶ Added code to set Boolean interlock signal to one when readout is out of limits
  - ✶ Added overall radial support upstream indicator to show interlock if any of the eight radial supports is out of limits
- Wrote PLC code to generate interlock based on the helium inlet and outlet temperatures
  - ✶ If temperature sensors' readback is out of limits, an interlock is generated and the magnet is ramped down
- Modified *Solenoid Radial and Axial Support – Expert* HMI screen to enable entering second thresholds for each radial support
- Populated all eight constant current source boards

Hall B – RICH II

Peter Bonneau, Tyler Lemon

- Refined ANSYS model for SHT35 sensor PCB
  - ✶ Replaced heat flow through faces of buffer driver with internally generated heat
  - ✶ Added convection to stagnant air for PCB substrate and buffer drivers
  - ✶ Reduced size of PCB substrate to match design

  - ✶ Refinements produced a small change in the distance from the drivers to the location where SHT35 sensors should be placed; from ~0.22" to ~0.21"
- Completed initial routing for SHT35 temperature and humidity sensor board layout
- Reviewed FPGA command engine routines and interface to the real-time scan engine
- Investigated methods of implementing the sensor cyclic redundancy check (CRC) into the real-time scan engine
- Completed first version of RICH Hardware Interlock System diagram and sbRIO hardware diagram

Hall B – SVT

Peter Bonneau

- Tested, successfully, hybrid flex circuit board temperature signal inputs to verify appropriate system interlocking operation after the installation of the cable quick-disconnect system

Hall C – CAEN Testing

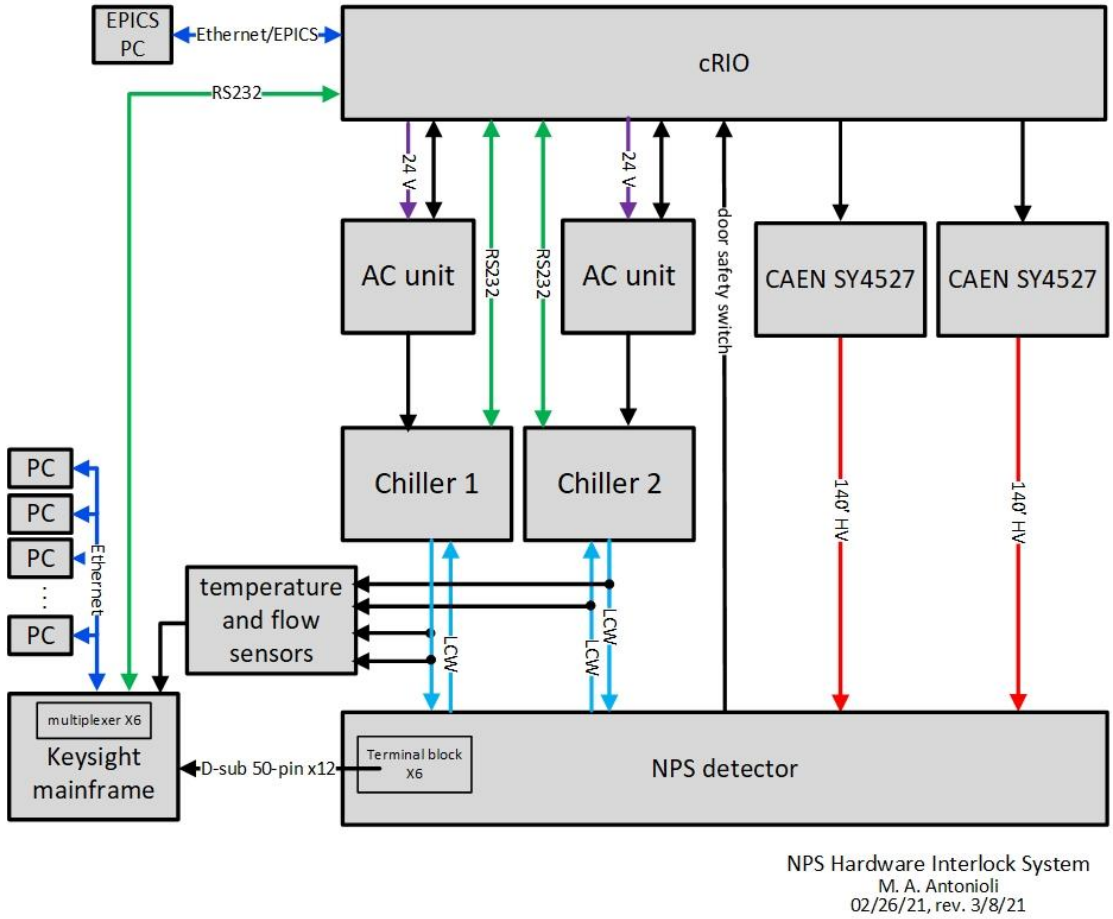
Mary Ann Antonioli, Aaron Brown, George Jacobs

- Completed voltage and current stability testing of CAEN 24-channel A1535 and A7435 modules; all testing complete
- Wrote Python code to generate plots for 24-channel A1535 and A7435 modules' voltage and current stability testing analysis

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, George Jacobs, Mindy Leffel, Tyler Lemon

- Reviewed remote AC power control module hardware requirements for interlocking crystal and electronic zone chillers
  - ✶ The chiller AC power interlock is controlled by a +24 V control voltage from the NI cRIO-9045 controller in the SHMS hut
  - ✶ When the chiller interlock trips, the 24 V control voltage is removed, disabling the chiller
  - ✶ The Bi-Ra AC power units used in the other DSG hardware interlock systems are no longer available
  - ✶ The Lowell Manufacturing model RPC-20-SCD remote power control module meets the requirements for this application and can be used as a replacement for the other DSG hardware interlock systems
- Developing CSS-BOY screen to turn on/off channels for all CAEN modules
  - ✶ Wrote Python script to turn on/off all channels of all modules in both crates
  - ✶ Wrote Javascript to turn on/off all channels of each module
- Completed Hardware Interlock System block diagram



NPS Hardware Interlock System block diagram

EIC

Brian Eng

- Developing list of CY2021 goals, which need to be prioritized and milestoned